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EXAMINER	
RODRIGUEZ, GLENDA P	
ART UNIT	**PAPER NUMBER**
2651	2

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/927,662	Applicant(s) SHELL ET AL.	
	Examiner Glenda P. Rodriguez	Art Unit 2651	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-11,14-18 and 20* is/are rejected.

7)☒ Claim(s) *12, 13 and 19* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 1, 4-10, 16, 17 and 20 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abbot et al. (US Patent No. 5, 341, 259) in view of Cheung et al. (US Patent No. 5, 442, 498).

Regarding Claims 1 and 16, Abbot et al. teach an apparatus comprising:

A sampler circuit configured to generate a digital signal in response to a pre-amplified signal (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 10, Lines 12-19);

And a filter circuit is configured to

(i) Improve signal to noise ratio (SNR) (Pat. No. 5, 341, 259; Col. 36, Lines 52-65)

(ii) Reject DC offset errors (Pat. No. 5, 341, 259; Col. 28, Lines 4-53).

Abbot et al. fail to teach that the filter circuit generates a track ID signal. However, this feature is well known in the art as disclosed by Cheung et al., wherein it teaches hat the filter circuit generates a track ID signal (Pat. No. 5, 442, 498; Col. 2, Line 66 to Col. 3, Line 12 and Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in

order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Method claim 17 is drawn to the method of using the corresponding apparatus claimed in claims 1 and 16. Therefore method claim 17 corresponds to apparatus claims 1 and 16 and is rejected for the same reasons of obviousness as used above.

Regarding Claim 4, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. further teach wherein said filter circuit is immune to DC offsets and shifts from thermal asperities (Pat. No. 5, 341, 249; Col. 36, Lines 52-65).

Regarding Claim 5, Abbot et al. teach all the limitations of Claim 1. Cheung et al. further teach wherein the filter circuit is further configured to attenuate high frequencies (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 6, Abbot et al. teach all the limitations of Claim 1. Cheung et al. further teach wherein the filter circuit is further configured to reject low frequencies (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 7, Abbot et al. teach all the limitations of Claim 1. Cheung et al. further teach wherein filter circuit is further configured to closely match said digital signal

(Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 20, Abbot et al. teach all the limitations of Claim 17. Cheung et al. further teach wherein the filter circuit is further configured to attenuate high frequencies and to reject low frequencies (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 8, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. further teach wherein the sampler comprises:

A voltage gain amplifier configured to receive said pre-amplified signal (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19);

A magneto-resistive head asymmetry correction circuit to said voltage gain amplifier (Pat. No. 5, 341, 259; Col. 9, Line 8-34);

A continuous time filter coupled to said magnetic-resistive asymmetry correction circuit (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19);

An offset cancellation circuit coupled to said continuous time filter (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19);

And an analog to digital conversion circuit configured to generate said digital signal and coupled to said offset cancellation circuit (Pat. No. 5, 341, 259; Col. 9, Lines 20-34 and Col. 9, Line 66 to Col. 10, Line 19).

Regarding Claim 9, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Cheung et al. further teach a filter circuit comprising: A digital filter circuit configured to generate a filtered track ID signal Pat. No. 5, 442, 498; Col. 5, Lines 30-53); A track ID decoder configured to generate said track ID signal in response to said filtered track ID signal (Pat. No. 5, 442, 498; Col. 5, Lines 30-53. Cheung et al. teach that the demodulator contains a decoder which decodes the track ID signal); A position error signal (PES) filter configured to generate a filtered PES signal in response to said digital signal and a PES demodulator configured to generate a PES signal in response to said filtered PES signal (Pat. No. 5, 442, 498; Col. 5, Lines 30-53). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al.'s invention in order to remove noise and harmonic that can cause PES and phase jitter (which in known to an artisan of ordinary skill in the art to be DC offset errors).

Regarding Claim 10, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. further teach a read channel circuit configured to generate a read

data signal response to said digital data signal (Pat. No. 5, 341, 249; Col. 9, Line 9 to Col. 10, Line 19).

Claims 2, 11 and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abbot et al. and Cheung et al. as applied to claim1 and 17, respectively above, and further in view of Izumi et al. (US Patent No. 6, 160, 673).

Regarding Claims 2 and 18, Abbot et al. and Cheung et al. teach all the limitations of Claims 1 and 16, respectively. Abbot et al. and Cheung et al. fail to teach wherein the filter circuit is configured to implement simple multiplication coefficients. However, this feature is well known in the art as disclosed by Izumi et al., wherein it teaches the filter circuit is configured to implement simple multiplication coefficients (Pat. No. 6, 160, 673; Col. 11, Line 66 to Col. 12, Line 47). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, in order to equalize the waveform.

Regarding Claim 11, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. and Cheung et al. fail to teach a filter circuit that comprises: one or more delay elements configured to delay said digital signal; and a summation circuit configured to perform summation of said delayed digital signals and provide an output filtered signal. However, this feature is well known in the art as disclosed by Izumi et al. (US Patent No. 6, 160, 673; Fig. 6, Element 63). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, in order to equalize the waveform.

Claims 14 and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Abbot et al. and Cheung et al. as applied to claim 1 above, and further in view of Yang (US Patent No. 6, 590, 728).

Regarding Claim 14, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. and Cheung et al. fail to teach wherein said track ID signal comprises a servo track ID signal. However, this feature is well known in the art as disclosed by Yang, wherein it teaches a said track ID signal comprises a servo track ID signal (Pat. No. 6, 590, 728; Col. 3, Line 57-Col. 4, Line 14). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al. and Cheung et al.'s invention in order to compensate for errors from the servo bursts.

Regarding Claim 15, Abbot et al. and Cheung et al. teach all the limitations of Claim 1. Abbot et al. and Cheung et al. fail to teach wherein a servo track ID filter is configured to generate the track ID signal in response to the digital signal. However, this feature is well known in the art as disclosed by Yang et al., wherein it teaches a servo track ID filter is configured to generate the track ID signal in response to the digital signal (Pat. No. 6, 590, 728; Col. 3, Line 57-Col. 4, Line 14 to Col. 4, Line 47-Col. 5, Line 7). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al. and Cheung et al.'s invention in order to compensate for errors from the servo bursts.

Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Abbot et al. and Cheung et al. as applied to claim 1 above, and further in view of Shimoda (US

Patent No. 6, 122, 120). Abbot et al. and Cheung et al. teach all the limitations of Claim 3. Abbot et al. and Cheung et al. fail to teach wherein the filter circuit is configured to implement multiplication coefficients of one. However, this feature is well known in the art as disclosed by Shimoda, wherein it teaches the filter circuit is configured to implement multiplication coefficients of one (Pat. No. 6, 122, 120; Fig. 8, Element 66, wherein it teaches 2 delays being multiplied by a coefficient of one.). It would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to modify Abbot et al. and Cheung et al.'s invention in order to equalize the signal (Pat. No. 6, 122, 120; Col. 7, Lines 16-57).

Allowable Subject Matter

Claims 12, 13 and 19 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Glenda P. Rodriguez whose telephone number is (703)305-8411. The examiner can normally be reached on Monday thru Thursday: 7:00-5:00; alternate Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Hudspeth can be reached on (703)308-4825. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

gpr
March 15, 2004.

DAVID HUDSPETH
SUPERVISORY PATENT EXAMINER
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